

SPECIFICATION

PART NO. : OEL9M0078-Y-E

OLED
132X16 **1.45"**

This specification maybe changed without any notice in order to improve performance or quality etc.

Please contact TRULY Semiconductors LTD. OLED R&D department for update specification and product status before design for this product or release the order.

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REVISION HISTORY

Rev.	Contents	Date
1.0	Initial release	2011-10-10

n PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	1.45	Inch
2	Resolution	132(H) x 16(V)	Lines
3	Active Area	36.412 (W) x 4.62(H)	mm
4	Outline Dimension (Panel)	43.06(W) x 11.75(H)	mm
5	Pixel Pitch	0.276(W) x 0.29(H)	mm
6	Pixel Size	0.256(W) x 0.27(H)	mm
7	Driver IC	SSD1305T7R1	-
8	Display Color	Yellow	-
8	Grayscale	1	-
9	Interface	Parallel / Serial/ I2C	-
10	IC package type	TCP	-
11	Thickness	1.6	mm
12	Weight	<1.7	g
13	Duty	1/16	-

n ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, $V_{SS} = 0V$

($T_a = 25^{\circ}C$)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	-0.3	-	4.0	V
	Driving	V_{CC}	0	-	16.0	V
Operating Temperature		T_{op}	-30	-	80	$^{\circ}C$
Storage Temperature		T_{st}	-40	-	85	$^{\circ}C$
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

n ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Unless otherwise specified, $V_{SS} = 0V$, $V_{DD} = 2.4V$ to $3.5V$ ($T_a = 25^{\circ}C$)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	2.4	3.0	3.5	V
	Operating	V_{CC}	7.0	11.0	15.0	V
Input Voltage	High Voltage	V_{IH}	$0.9 \times V_{DD}$	-	V_{DD}	V
	Low Voltage	V_{IL}	V_{SS}	-	$0.1 \times V_{DD}$	V
Output Voltage	High Voltage	V_{OH}	$0.8 \times V_{DD}$	-	V_{DD}	V
	Low Voltage	V_{OL}	V_{SS}	-	$0.2 \times V_{DD}$	V

◆ AC Characteristics

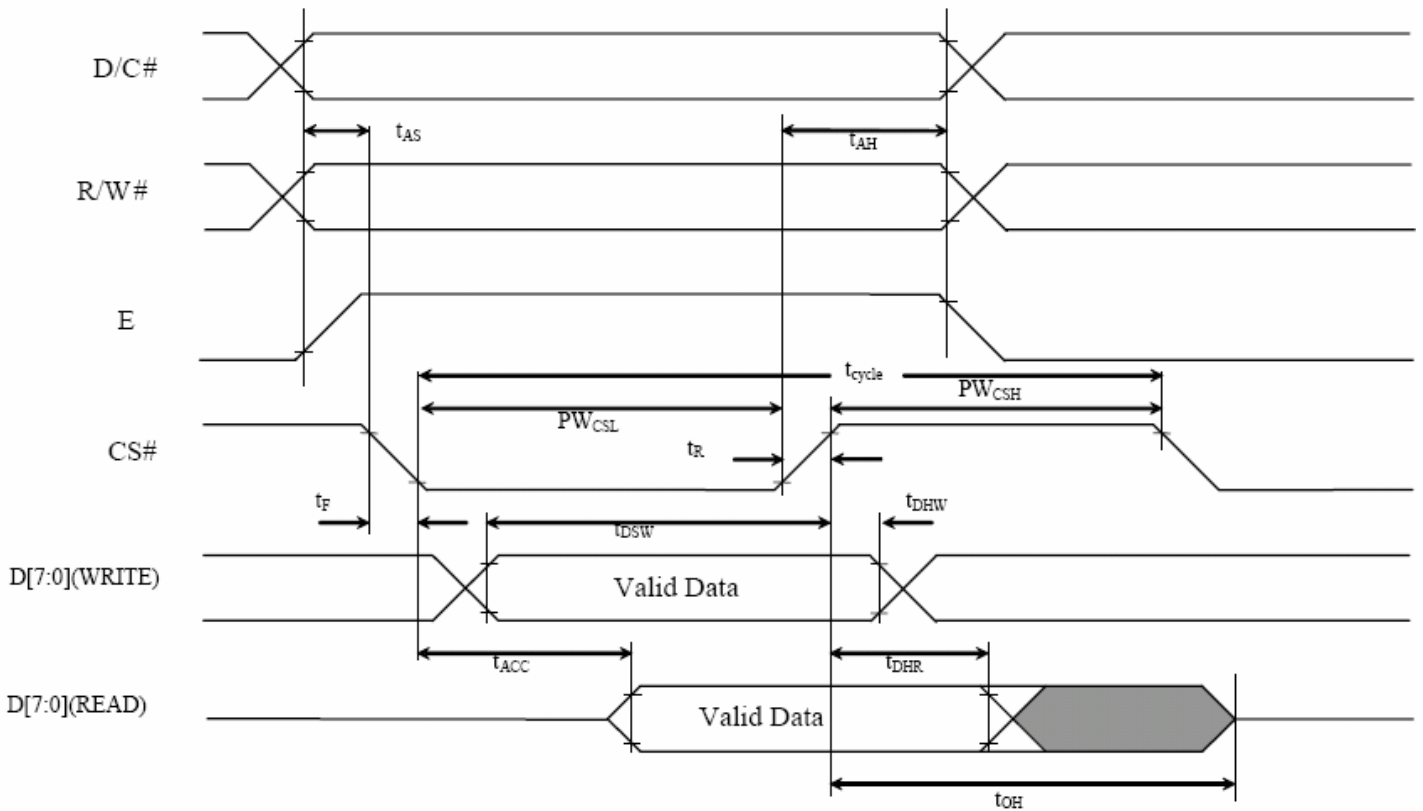
Use 8080/6800-Series MPU Parallel Interface or Serial Interface

1. 6800 Series MPU Parallel Interface

6800-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = V_{DD}$, $T_A = 25^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



6800-series MCU parallel interface characteristics

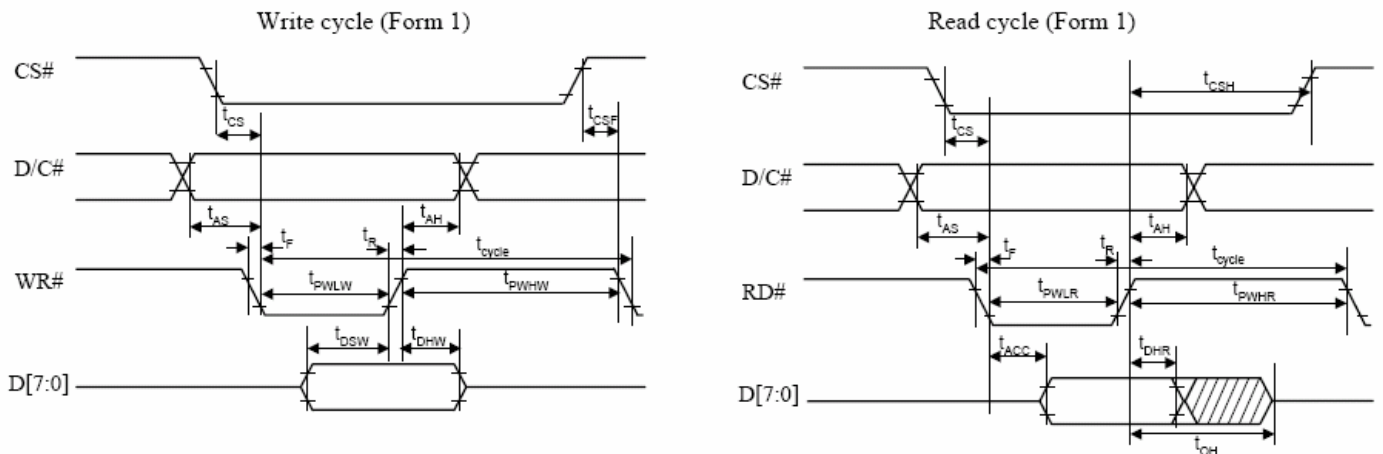
2. 8080 Series MPU Parallel Interface

8080-Series MCU Parallel Interface Timing Characteristics

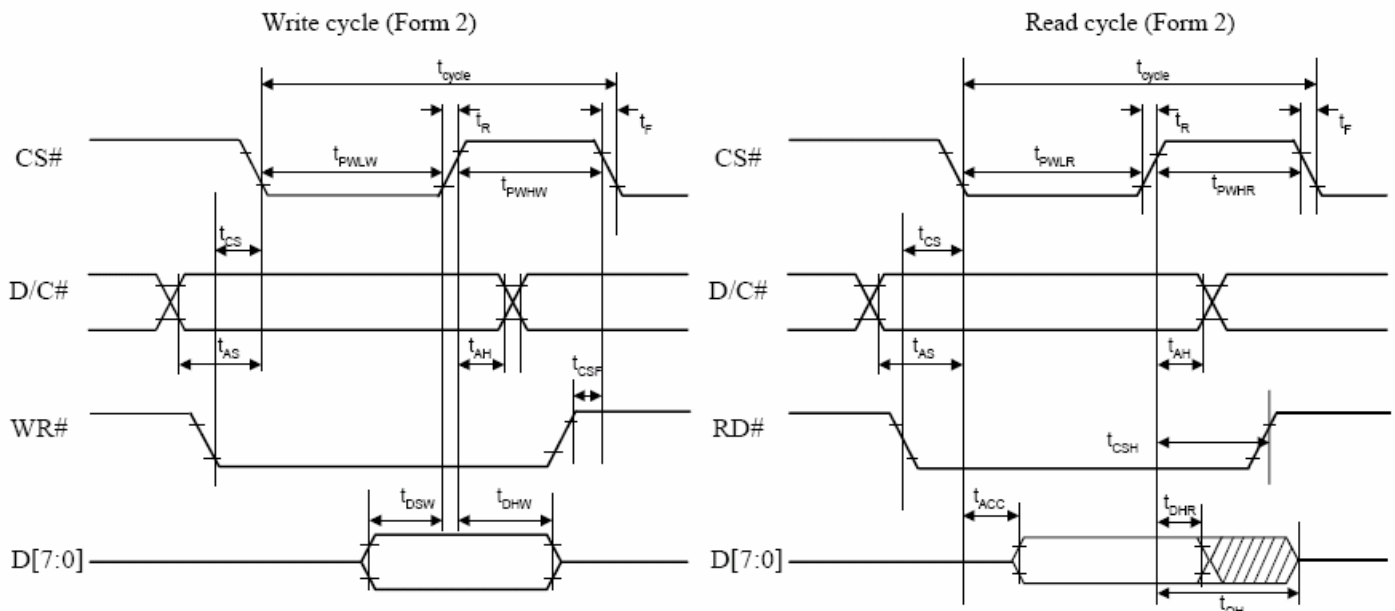
($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = V_{DD}$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)



8080-series parallel interface characteristics (Form 2)



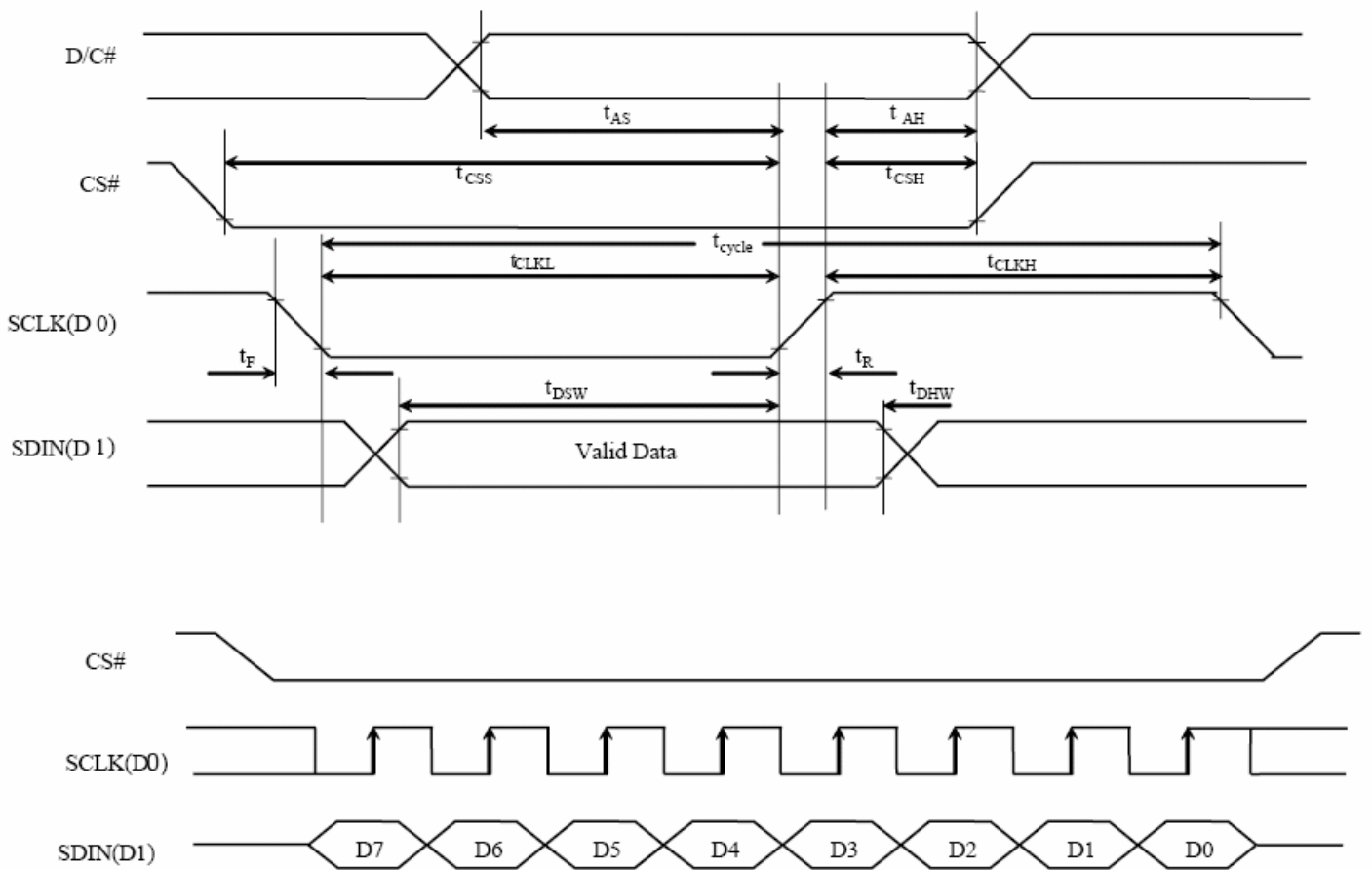
3. Serial Interface

Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = V_{DD}$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Serial interface characteristics



n TIMING OF POWER SUPPLY

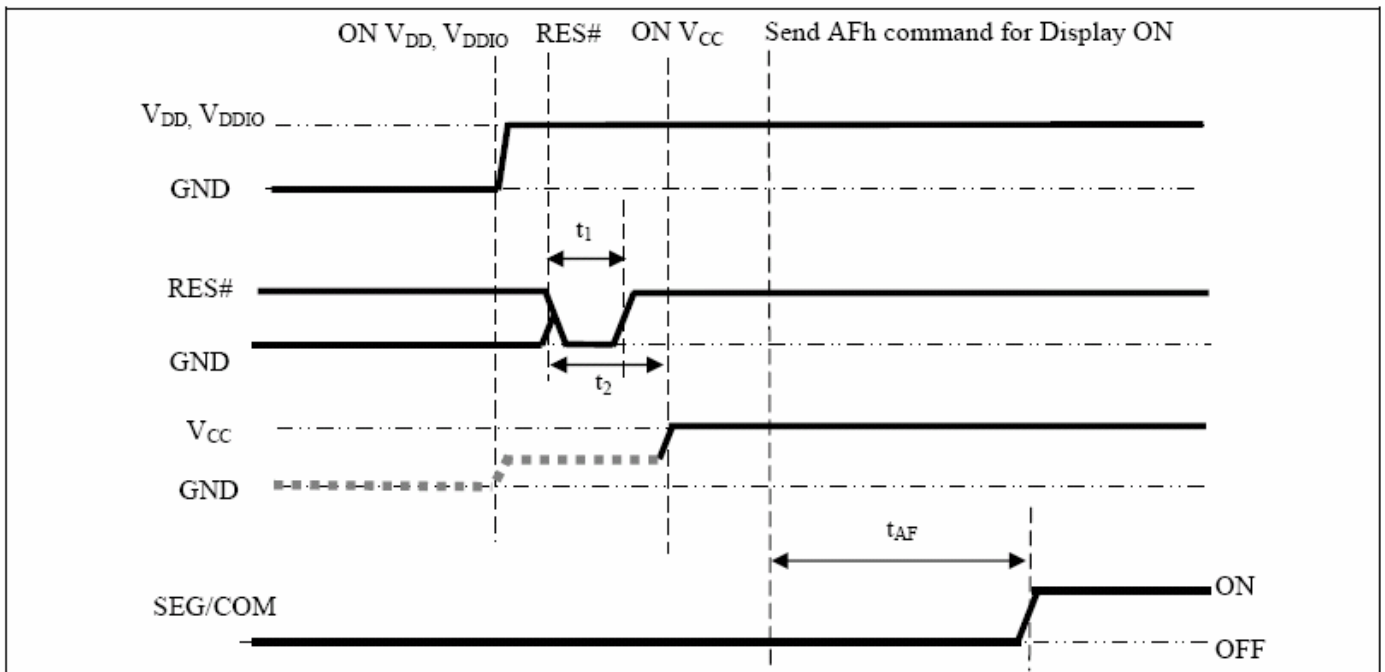
Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1305 (assume V_{DD} and V_{DDIO} are at the same voltage level).

Power ON sequence:

1. Power ON V_{DD} , V_{DDIO} .
2. After V_{DD} , V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3 μ s (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 μ s (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

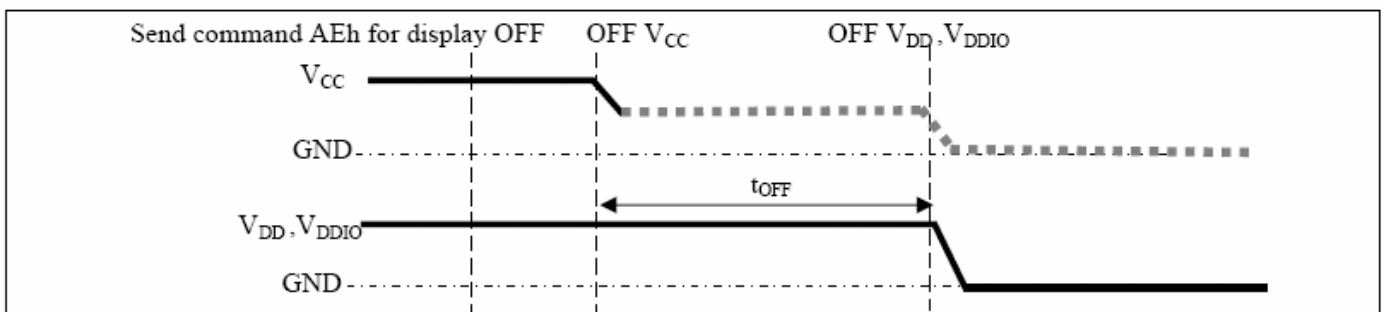
Figure 1 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{DD} , V_{DDIO} . (where Minimum t_{OFF} =0ms, Typical t_{OFF} =100ms)

Figure 2 : The Power OFF sequence



Note:

⁽¹⁾ Since an ESD protection circuit is connected between V_{DD} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 1 and Figure 2.

⁽²⁾ V_{CC} should be kept float (disable) when it is OFF.

n ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	85	100*	-	cd /m ²	Yellow
Power Consumption		P	-	20	30	mW	30% pixels ON L=100cd/m ²
Frame Frequency		Fr	-	100	-	Hz	
Color Coordinate	Yellow	CIE x	0.42	0.46	0.50	CIE1931	Darkroom
		CIE y	0.47	0.51	0.55		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	40,000	-	-	Hours	L=100cd/m ²

Note:

1. **100cd/m²** is base on V_{DD}=3.0V, V_{CC}=11.0V, contrast command setting 0x1F;
2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed)
(The initial value should be closed to the typical value after adjusting.)

n INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC	No connection
2	VCC	High voltage supply for OLED panel
3	VCOMH	High level voltage output of COM signal
4	IREF	Current reference pin
5	D7	Data bus or High impedance in Serial mode
6	D6	Data bus or High impedance in Serial mode
7	D5	Data bus or High impedance in Serial mode
8	D4	Data bus or High impedance in Serial mode
9	D3	Data bus or High impedance in Serial mode
10	D2	Data bus or left open in Serial mode
11	D1	Data bus or as SDIN in Serial mode
12	D0	Data bus or as SCLK in Serial mode
13	E/RD#	MCU interface input pin
14	R/W#	MCU interface input pin
15	D/C#	Data/Command data control pin
16	RES#	MCU control or RC for low pulse start up
17	CS#	The chip select pin. Low is enabled
18	NC	No connection
19	BS2	MCU bus interface selection pins
20	BS1	
21	VDD	Logic voltage supply for IC
22	NC	No connection
23	NC	No connection
24	NC	No connection
25	VBREF	This is a reserved pin, It should be kept NC.
26	NC	No connection
27	FB	This is a reserved pin, It should be kept NC.
28	Vddb	This is a reserved pin. It must be connected to VDD.
29	GDR	This is a reserved pin, It should be kept NC.
30	VSS	Ground
31	NC	No connection

MCU Bus Interface Pin Selection

Pin name	8080-parallel(8bit)	6800-parallel(8bit)	Serial Interface	I2C Interface
BS1	1	0	0	1
BS2	1	1	0	0

Note: 0 is connected to Vss
1 is connected to VDD.

n COMMAND TABLE

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	20	0	0	1	0	0	0	0	0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0	A[1:0]	*	*	*	*	*	*	A ₁	A ₀		
0	21	0	0	1	0	0	0	0	1	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-131d, (RESET=0d) B[7:0]: Column end address, range : 0-131d, (RESET =131d)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	B[7:0]	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	
0	22	0	0	1	0	0	0	1	0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀		
0	0	B[2:0]	*	*	*	*	B ₂	B ₁	B ₀		
0	40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000b during RESET.
0	81	1	0	0	0	0	0	0	1	Set Contrast Control For BANK0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	82	1	0	0	0	0	0	1	0	Set Brightness For Area Color Banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT)	Set current drive pulse width of BANK0, Color A, B and C. BANK0: X[5:0] = 31... 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b)
0	X[5:0]	*	*	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀		
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[5:0]	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
											Note (1) Color D pulse width is fixed at 64 clocks pulse.

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A ₇ B ₇ C ₇ D ₇	0 A ₆ B ₆ C ₆ D ₆	0 A ₅ B ₅ C ₅ D ₅	1 A ₄ B ₄ C ₄ D ₄	0 A ₃ B ₃ C ₃ D ₃	0 A ₂ B ₂ C ₂ D ₂	1 A ₁ B ₁ C ₁ D ₁	0 A ₀ B ₀ C ₀ D ₀	Set Bank Color of BANK1 to BANK16 (PAGE0)	Set the bank color of BANK1~BANK16 to any one of the 4 colors : A, B, C and D . A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK1 A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK2 : : : D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK15 D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK16
0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[7:0]	1 A ₇ B ₇ C ₇ D ₇	0 A ₆ B ₆ C ₆ D ₆	0 A ₅ B ₅ C ₅ D ₅	1 A ₄ B ₄ C ₄ D ₄	0 A ₃ B ₃ C ₃ D ₃	0 A ₂ B ₂ C ₂ D ₂	1 A ₁ B ₁ C ₁ D ₁	1 A ₀ B ₀ C ₀ D ₀	Set Bank Color of BANK17~BANK32 (PAGE1)	Set the bank color of BANK17~BANK32 to any one of the 4 colors: A, B, C and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK17 A[3:2] : 00b, 01b, 10b, or 1b1 for Color = A, B, C or D of BANK18 : : : D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK31 D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK32
0	A0/A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map	X[0]=0b: column address 0 is mapped to SEG0 (RESET) X[0]=1b: column address 131 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X ₀	Entire Display ON	X ₀ =0b: Resume to RAM content display (RESET) Output follows RAM content X ₀ =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display	X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel X[0]=1b: inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[5:0]	1 *	0 *	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET=111111b (i.e. 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	AA	1	0	1	0	1	0	1	0	Reserved	Reserved
0 0 0 0	AB A[3:0] B[7:0] C[7:0]	1 * B ₇ C ₇	0 * B ₆ C ₆	1 * B ₅ C ₅	0 * B ₄ C ₄	1 A ₃ C ₃	0 A ₂ C ₂	1 A ₁ C ₁	1 A ₀ C ₀	Dim mode setting	A[3:0] : Reserved (set as 0000b) B [7:0] : Set contrast for BANK0, valid range 0-255d, please refer to command 81h C [7:0] : Set brightness for color bank, valid range 0-255d, please refer to command 82h

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A ₀	Master Configuration	A[0]=0b, Select external V _{CC} supply (RESET) A[0]=1b, Select internal DC-DC voltage converter Note (1) Refer to Section 8.11 for DC-DC converter details (2) The DC-DC converter must be enabled by the following command: ADh ; Master Configuration 8Fh ; Enable internal DC-DC AFh or ACh ; Display ON
0	AC AE AF	1	0	1	0	1	1	A ₁	A ₀	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0	B0~B7	1	0	1	1	0	X ₂	X ₁	X ₀	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
0	C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N -1] X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset	Set vertical shift by COM from 0~63. The value is reset to 00h after RESET.
0	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F _{OSC} . Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b Range:0000b~1111b Frequency increases as setting value increases. Refer to section 10.1.23 for details.
0 0	D8	1 0	1 0	0 X ₅	1 X ₄	1 0	0 X ₂	0 0	0 X ₀	Set Area Color Mode ON/OFF & Low Power Display Mode	X[5:4]= 00b (RESET) : monochrome mode X[5:4]= 11b Area Color enable X[2]=0b and X[0]=0b: Normal power mode(RESET) X[2]=1b and X[0]=1b: Set low power display mode
0 0	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry A[7:4] : Phase 2 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry

Fundamental Command Table																							
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description												
00	DA	1	1	0	1	1	0	1	0	Set COM Pins Hardware Configuration	X[4]=0b, Sequential COM pin configuration X[4]=1b(RESET), Alternative COM pin configuration X[5]=0b(RESET), Disable COM Left/Right remap X[5]=1b, Enable COM Left/Right remap Please refer to Table 10-3 for details.												
00	DB A[5:2]	1 0	1 0	0 A ₅	1 A ₄	1 A ₃	0 A ₂	1 0	1 0	Set V _{COMH} Deselect Level	<table border="1"> <thead> <tr> <th>A[5:2]</th> <th>Hex code</th> <th>V_{COMH} deselect level</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>00h</td> <td>~ 0.43 x V_{CC}</td> </tr> <tr> <td>1101b</td> <td>34h</td> <td>~ 0.77 x V_{CC} (RESET)</td> </tr> <tr> <td>1111b</td> <td>3Ch</td> <td>~ 0.83 x V_{CC}</td> </tr> </tbody> </table>	A[5:2]	Hex code	V _{COMH} deselect level	0000b	00h	~ 0.43 x V _{CC}	1101b	34h	~ 0.77 x V _{CC} (RESET)	1111b	3Ch	~ 0.83 x V _{CC}
A[5:2]	Hex code	V _{COMH} deselect level																					
0000b	00h	~ 0.43 x V _{CC}																					
1101b	34h	~ 0.77 x V _{CC} (RESET)																					
1111b	3Ch	~ 0.83 x V _{CC}																					
00	E0	1	1	1	0	0	0	0	0	Enter Read Modify Write	Enter the Read Modify Write mode. Details please refer to section 10.1.28.												
00	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation												
00	EE	1	1	1	0	1	1	1	0	Exit Read Modify Write	Exit the Read Modify Write mode (Please refer to command E0h)												

Graphic Acceleration Command Table																																					
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																										
0	26/27	0	0	1	0	0	1	1	X ₀	Horizontal Scroll Setup	X[0]=0, Right Horizontal Scroll X[0]=1, Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> C[2:0] : Set time interval between each scroll step in terms of frame frequency <table border="1"> <tr> <td>000b – 6 frames</td> <td>100b – 3 frames</td> </tr> <tr> <td>001b – 32 frames</td> <td>101b – 4 frames</td> </tr> <tr> <td>010b – 64 frames</td> <td>110b – 2 frame</td> </tr> <tr> <td>011b – 128 frames</td> <td>111b – Invalid</td> </tr> </table> D[2:0] : Define end page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> The value of D[2:0] must be larger or equal to B[2:0]	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5		000b – 6 frames	100b – 3 frames	001b – 32 frames	101b – 4 frames	010b – 64 frames	110b – 2 frame	011b – 128 frames	111b – Invalid	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
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001b – PAGE1	100b – PAGE4	111b – PAGE7																																			
010b – PAGE2	101b – PAGE5																																				
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀																												
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀																												
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀																												
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀																												
0	29/2A	0	0	1	0	1	0	X ₁	X ₀	Continuous Vertical and Horizontal Scroll Setup	X ₁ X ₀ =01b : Vertical and Right Horizontal Scroll X ₁ X ₀ =10b : Vertical and Left Horizontal Scroll A[2:0] : Set number of column scroll offset 000b No horizontal scroll 001b Horizontal scroll by 1 column 010b Horizontal scroll by 2 columns 011b Horizontal scroll by 3 columns 100b Horizontal scroll by 4 columns Other values are invalid. B[2:0] : Define start page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> C[2:0] : Set time interval between each scroll step in terms of frame frequency <table border="1"> <tr> <td>000b – 6 frames</td> <td>100b – 3 frames</td> </tr> <tr> <td>001b – 32 frames</td> <td>101b – 4 frames</td> </tr> <tr> <td>010b – 64 frames</td> <td>110b – 2 frame</td> </tr> <tr> <td>011b – 128 frames</td> <td>111b – Invalid</td> </tr> </table> D[2:0] : Define end page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table> The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0]=3Fh refer to offset =63 rows	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5		000b – 6 frames	100b – 3 frames	001b – 32 frames	101b – 4 frames	010b – 64 frames	110b – 2 frame	011b – 128 frames	111b – Invalid	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																																			
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010b – PAGE2	101b – PAGE5																																				
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀																												
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀																												
0	C[2:0]	*	*	*	*	*	C ₂	C ₁	C ₀																												
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀																												
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀																												

Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	<p>Stop scrolling that is configured by command 26h/27h/29h/2Ah.</p> <p>Note ⁽¹⁾ After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.</p>
0	2F	0	0	1	0	1	1	1	1	Activate scroll	<p>Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences:</p> <p>Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh.</p> <p>For example, if “26h; 2Ah; 2Fh.” commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.</p>
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	<p>A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0). [RESET = 0]</p> <p>B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64]</p> <p>Note ⁽¹⁾ A[5:0]+B[6:0] <= MUX ratio ⁽²⁾ B[6:0] <= MUX ratio ^(3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] ^(3b) Set Display Start Line (X5X4X3X2X1X0 of 40h~7Fh) < B[6:0] ⁽⁴⁾ The last row of the scroll area shifts to the first row of the scroll area. ⁽⁵⁾ For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls Please refer to Figure 10-14 for details.</p>
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		

n INITIALIZATION CODE

```
void InitOLED_SSD1305(void)
{
    MainOLED_WCom(0xAE);    //DOT MARTIX DISPLAY OFF

    MainOLED_WCom(0x40);    //SET DISPLAY START LINE(40H-7FH)

    MainOLED_WCom(0x81);    //CONTARST CONTROL(00H-0FFH)
    MainOLED_WCom(CONTRAST);

    MainOLED_WCom(0xA0);    //SET SEGMENT RE-MAP(0A0H-0A1H)
    MainOLED_WCom(0xA4);    //ENTIRE DISPLAY OFF(0A4H-0A5H)
    MainOLED_WCom(0xA6);    //SET NORMAL DISPLAY(0A6H-0A7H)

    MainOLED_WCom(0xA8);    //SET MULTIPLEX RATIO 64
    MainOLED_WCom(0x0F);

    MainOLED_WCom(0xB0);    // Set Page Start Address (PAGE0~PAGE7)
    //for Page Addressing Mode

    MainOLED_WCom(0xC8);    //COM SCAN COM1-COM64(0C8H,0C0H)

    MainOLED_WCom(0xD3);    //SET DISPLAY OFFSET(00H-3FH)
    MainOLED_WCom(0x00);

    MainOLED_WCom(0xD5);    //SET FRAME FREQUENCY
    MainOLED_WCom(0x51);

    MainOLED_WCom(0xD9);    //SET PRE_CHARGE PERIOD
    MainOLED_WCom(0x22);

    MainOLED_WCom(0xDA);    //COM PIN CONFIGURATION(02H,12H)
    MainOLED_WCom(0x12);

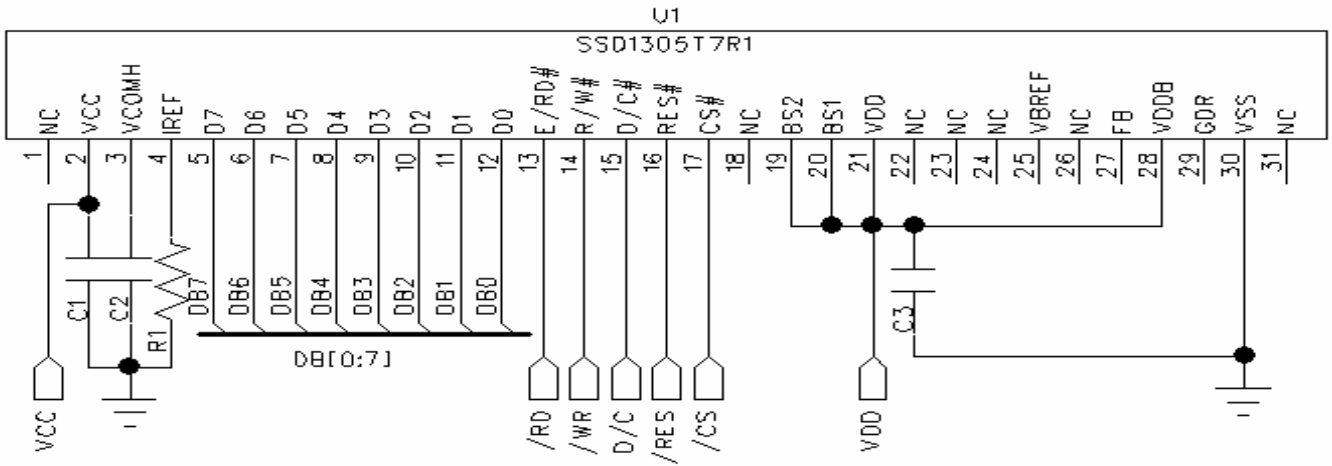
    MainOLED_WCom(0xDB);    //SET VCOM DESELECT LEVEL(035H)
    MainOLED_WCom(0x35);

    Delayms(10);

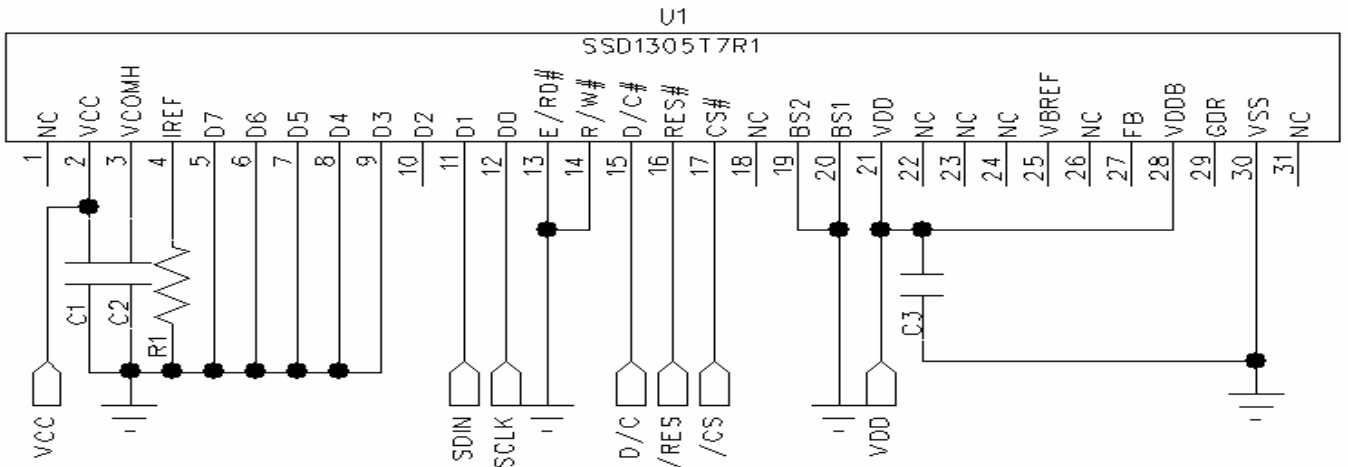
    MainOLED_WCom(0xAF);    //DSPLAY ON
}
```

SCHEMATIC EXAMPLE

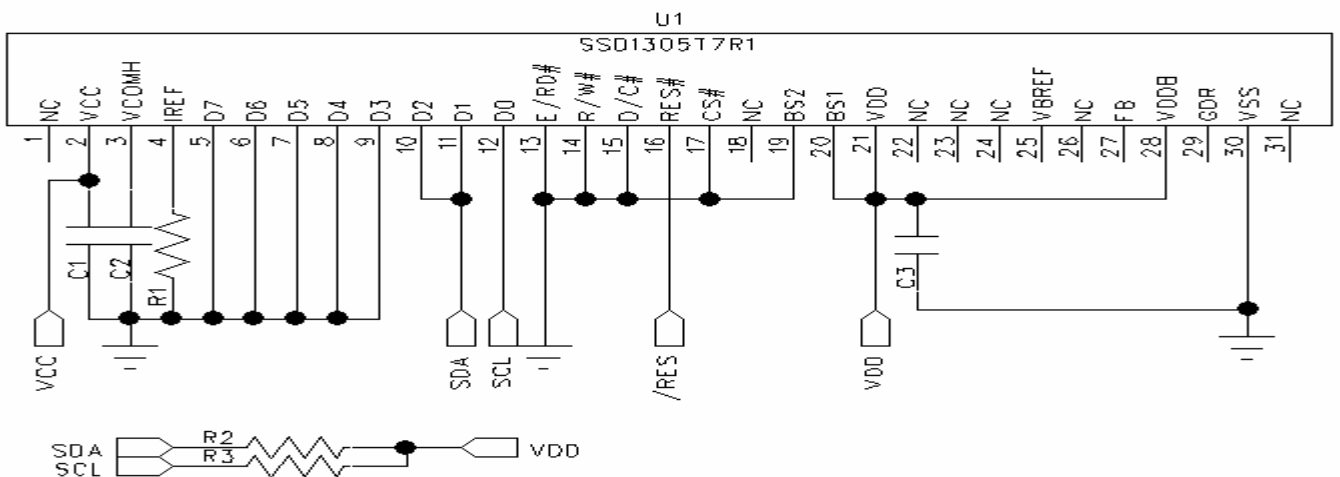
◆8080 parallel Interface Application Circuit:



◆Serial Interface Application Circuit:



◆IIC Interface Application Circuit:



NOTE:

1. $R1 = (V_{CC} - 3)V / 10\mu A = (11 - 3)V / 10\mu A \approx 800K\Omega$, $C1 = C2 = C3 = 4.7\mu F$, $R2 = R3 = 10K$;
2. The V_{CC} should connect an external voltage;
3. In Serial interface mode, the read function is not possible.

n RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		85±.2°C , 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		80±2°C , 96 hours	
Low Temperature Storage (LTS)		-40±2°C , 200 hours	
Low Temperature Operating (LTO)		-30±2°C , 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3°C , 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2°C ~ 25°C ~ 70±2°C (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

- Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.
 2) The HTHHS test is requested the Pure Water(Resistance > 10MΩ).
 3) The test should be done after 2 hours of recovery time in normal environment.

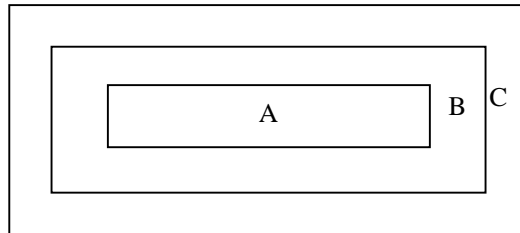
OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

- 1 Major defect : The defect that greatly affect the usability of product.
- 2 Minor defect : The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

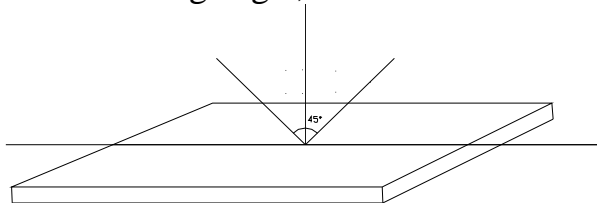
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

- 1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5 °C.



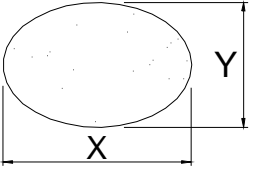
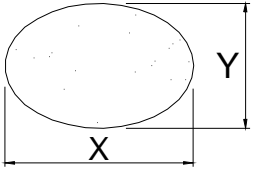
- 2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5 °C.

◆Inspection Criteria

- 1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

- 2 Minor Defect : AQL= 1.5

Item	Criterion			
Spot Defect (dimming and lighting spot)	Size (mm)		Accepted Qty	
			$\Phi \leq 0.07$	Ignored
			$0.07 < \Phi \leq 0.10$	3
			$0.10 < \Phi \leq 0.15$	1
			$0.15 < \Phi$	0
Note : $\Phi = (x + y) / 2$				
Line Defect (dimming and lighting line)	L (Length) : mm	W (Width) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignored	
	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	Ignored
	$L \leq 2.0$	$0.03 < W \leq 0.05$	1	
	/	$0.05 < W$	As spot defect	
Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm				
Polarizer Stain	Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.			
Polarizer Scratch	1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.			
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :			
	L (Length) : mm	W (Width) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignore	
	$3.0 < L \leq 5.0$	$0.02 < W \leq 0.04$	2	Ignore
	$L \leq 3.0$	$0.04 < W \leq 0.06$	1	
/	$0.06 < W$	0		
Polarizer Air Bubble	Size		Area A + Area B	Area C
			$\Phi \leq 0.20$	Ignored
			$0.20 < \Phi \leq 0.30$	2
			$0.30 < \Phi \leq 0.50$	1
			$0.50 < \Phi$	0

Glass Defect (Glass Chipped)	1. On the corner	(mm)	<table border="1"> <tr> <td>x</td> <td>≤ 1.5</td> </tr> <tr> <td>y</td> <td>≤ 1.5</td> </tr> <tr> <td>z</td> <td>$\leq t$</td> </tr> </table>	x	≤ 1.5	y	≤ 1.5	z	$\leq t$
	x	≤ 1.5							
	y	≤ 1.5							
	z	$\leq t$							
2. On the bonding edge	(mm)	<table border="1"> <tr> <td>x</td> <td>$\leq a / 4$</td> </tr> <tr> <td>y</td> <td>$\leq s / 3 \ \&\leq 0.7$</td> </tr> <tr> <td>z</td> <td>$\leq t$</td> </tr> </table>	x	$\leq a / 4$	y	$\leq s / 3 \ \&\leq 0.7$	z	$\leq t$	
x	$\leq a / 4$								
y	$\leq s / 3 \ \&\leq 0.7$								
z	$\leq t$								
3. On the other edges	(mm)	<table border="1"> <tr> <td>x</td> <td>$\leq a / 8$</td> </tr> <tr> <td>y</td> <td>≤ 0.7</td> </tr> <tr> <td>z</td> <td>$\leq t$</td> </tr> </table>	x	$\leq a / 8$	y	≤ 0.7	z	$\leq t$	
x	$\leq a / 8$								
y	≤ 0.7								
z	$\leq t$								
Note: t: glass thickness ; s: pad width ; a: the length of the edge									
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted								
Pixel Size	The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec								
Luminance	Refer to the spec or the reference sample								
Color	Refer to the spec or the reference sample								

n CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module' s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆ **PRIOR CONSULT MATTER**

1. For TRULY standard products , we keep the right to change material ,process ... for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.